UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,060	03/19/2004	Takayuki Kondo	118944	8241

25944 7590 01/10/2006

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,060	KONDO, TAKAYUKI	
	Examiner	Art Unit	
	Lex Malsawma	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

2. The translation of priority document JP 2003-097972 has been considered and the previous rejection of claims 1-15, based primarily on Kondo (US 2004/0036078) and Feng (US 2005/0040432), has been withdrawn. However, all pending claims have been reconsidered in view of newly cited references.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation in claim 5 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. More specifically, none of the figures show the third layer being longer than that of the second layer, e.g., in Fig. 4, the third layer "E" is show to be equally long as the second layer "B".

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the

drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 11 and 12 are objected to because of the following informalities:

In claim 11, line two, "the one first metal" should read "the first metal", otherwise, there would be a lack of antecedent basis.

In claim 12, lines 2-4, "the one second" and "the one third" should read "the second" and "the third", respectively, otherwise, there would be a lack of antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-9, 11, 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by **Devries** (3,590,479).

Regarding claims 1, 6, 9, 11 and 13 :

Devries discloses (in Figs. 1-4) a transistor, comprising:

an insulating substrate (10/11) in Fig. 3;

a first metal film 6 disposed on the insulating substrate (Fig. 3);

a first layer 5 (Figs. 2-3), which is arranged on the first metal film 6 and which is made of an N-type semiconductor which is electrically coupled to the first metal film 6;

a second layer 4, which is disposed on the first layer 5 and which is made of a P-type semiconductor;

a third layer (3/1/13), which is disposed on the second layer and which is made of an N-type semiconductor (see Fig. 4);

a second metal film 7, which is disposed on the insulating substrate (10/11) in such a manner as not to be brought into contact with the first metal film 6, but which is brought into contact with the second layer 4 (see Fig. 3);

a third metal film 16 (Fig. 4) which is disposed on the insulating substrate in such a manner as not to be brought into contact with the first metal film 6 and the second metal film 7, but which is brought into contact with the third layer (3/1/13). NOTE: Although the third metal film 16 is not in direct physical contact with the insulating substrate, it is nevertheless disposed on the insulating substrate;

the first layer 5, the second layer 4, and the third layer (3/1/13) being formed so as to cross on the top surface of the first metal (Fig. 4), i.e., each of the first, second and third layers crosses a top surface of the first metal film 6;

the transistor being formed of a transistor that functions as a hetero-bipolar transistor (i.e., an NPN transistor);

a plurality of first layers being provided on the first metal film, and the second layer and the third layer being provided for each of the first layers (i.e., a plurality of NPN transistors are shown in Figs. 6-7, accordingly, Devries discloses a plurality of first, second and third layers provided on the first metal film 6, e.g., note the metal film connecting the two first n-type layers of each NPN transistor in Fig. 7); and

the first metal film 6, the second metal film 7, and the third metal film 16 do not intersect one another (Fig. 4). Therefore, Devries anticipates this claim.

Regarding claim 4:

Devries discloses the second layer 4 is formed on an entire top surface of the first layer 3 (Fig. 3-4), and the third layer 3/1/13 is formed on [at least] a part of an area of the top surface of the second layer 4 (Fig. 4); therefore, Devries anticipates this claim.

Regarding claims 2, 3, 5, 7, 8 and 14:

Initially, with respect to these claims, the elements recited in claim 1 will be referred to as follows:

the first layer would be layer "3/1/13", which is a collector (Fig. 4);

the second layer would remain layer "4", which is a base;

the third layer would be layer "5", which is an emitter;

the first metal film would be film "16", which functions as collector wiring;

the second metal film would remain film "7", which functions as base wiring; and

the third metal film would be film "6", which functions as emitter wiring.

Note that the claim language cannot exclude the word, "on", from being interpreted as "on a top side" or "on a bottom side", for example, insofar as these claims, Devries discloses a first metal film 16 disposed on [a top side of] the insulating substrate; a first layer "3/1/13" arranged on [a bottom side of] the first metal film 16, etc., i.e., even though some of the reference elements have been interchanged with respect to these claims, all elements and their relative locations (as currently recited/claimed) are disclosed by Devries.

Specifically regarding claim 5:

Devries disclose the first layer 3/1/13 and the second layer 4 being formed in a rectangular plate shape (note Figs. 5 and 7), and Devries shows (in Figs. 5 and 7) that the transistor structure has tapered sides, i.e., all four sides are tapered such that the first metal film 16 would have the shortest length in comparison to layers 1, 3, 4 and 5 (note Figs. 2 and 4). Accordingly, Devries further discloses the third layer 5 being formed in a rectangular shape, which is longer and narrower than that of the first layer 3/1/13 and the second layer 4 (see Figs. 2, 4, 7). Therefore, this claim is anticipated.

Specifically regarding claim 7:

Devries discloses the first layer, the second layer, and the third layer are formed of layers having tile-shapes, which are small tile-shaped semiconductor elements (note Fig. 7). It is noted that a "tile shape" could be square-shaped, rectangular-shaped, circular-shaped, etc.; furthermore, since "small" is relative, the tile-shaped elements disclosed by Devries could surely be referred to as being small.

Specifically regarding claim 8:

Devries discloses the tile-shaped elements being such that a collector electrode 16 (Fig. 4) is formed on a bottom surface of the first layer 3/1/13 (i.e., "top" and "bottom" are relative to a chosen frame of reference, and in this particular case, the structure in Fig. 4 would be viewed upside down), a base electrode 7 is formed in an area other than the area where the third layer 5 is provided on a top surface of the second layer 4, and an emitter electrode 6 is formed on a top surface of the third layer 5; and the collector electrode 16 in the tile-shaped elements being joined to the first metal film 16 (i.e., the collector electrode is the first metal film), the base electrode 7 being joined to the second metal film 7 (i.e. the base electrode is the second metal film), and the emitter electrode 6 being joined to the third metal film 6 (i.e., the emitter electrode is the third metal film).

Specifically regarding claim 14:

Devries discloses a portion of the second metal film 7, that is not coupled to the second layer 4 (Figs. 3-4) in the second metal film, is directly provided on the insulating substrate 10/11, and a portion of the third metal film 6, that is not coupled to the third layer 5 in the third metal film, being directly provided on the insulating substrate 10/11. Therefore, Devries anticipates these claims 2, 3, 5, 7, 8 and 14.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Devries** (3,590,479) in view of **Yanagisawa** (US 2003/0160266 A1).

Regarding claim 10:

Devries anticipates claims 1 and 9 but **lacks** specifying materials for the first, second and third layers, i.e., Devries lacks specifically disclosing gallium, arsenic and aluminum. Yanagisawa is **cited only to show** that gallium, arsenic and aluminum were well known and utilized in art hetero-bipolar transistors (HBT), similar to the transistor structure disclosed by Devries. In paragraphs 0004 and 0005, Yanagisawa discloses gallium, arsenic and aluminum (i.e., AlGaAs) are commonly utilized for HBTs. Since Devries does not specify materials, it would have been obvious to one of ordinary in the art to utilize gallium, arsenic and aluminum because Yanagisawa shows that it was common in the art to do so, i.e., given Devries, one of ordinary skill in the art would found it obvious to utilize any well known materials, such as those shown by Yanagisawa.

9. Claims 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Devries** (3,590,479) in view of **Sovero** (5,378,922).

Regarding claim 12:

Devries anticipates claims 1 and 11 but **lacks** a plurality of second layers being coupled by the second metal film; and a plurality of third layers being coupled by the third metal film. It is important to note that Devries discloses only one specific example for a circuit utilizing HBTs

of the disclosure, i.e., note Figs. 6-7 and Col. 4 (lines 12-18), wherein Devries discloses an example where the base of a second transistor (24) is connected to the collector of a first transistor (23), accordingly, in this example Devries discloses the second layer (base layer) of the second transistor is connected to the third layer (collector layer) of the first transistor. Sovero **teaches** it was well known in the art that a plurality of HBTs can be connected in parallel if so needed/desired (note Figs. 1-2). Sovero shows in such a circuit, the base layers (B) and the collector layers (C) are coupled to one another, respectively; and Sovero teaches such a circuit provides protection against "thermal runaway" for some specific applications (note Col. 1, line 40 to Col. 2, line 16). Given Sovero along with Devries' disclosure (in Col. 4, lines 15-17) that a large number of circuits, besides the example shown in Figs. 6-7, could be formed with the HBTs, it would have been obvious to one of ordinary skill in the art to modify Devries by specifically coupling a plurality of second layers (base layers) and a plurality of third layers (collector layers) because such a modification would provide a circuit comprising a plurality of HBTs connected in parallel that could protect against "thermal runaway" for some specific applications.

10. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Devries** (3,590,479) in view of **Malik** (US 2002/0155670 A1).

Regarding claim 15:

Devries anticipates claims 1 but **lacks** specifically incorporating the HBT into an electronic device comprising an optical interconnection circuit. Malik is **cited to show** it was well known in the art that HBTs are of great commercial interest for incorporation into electronic

devices for optical interconnection circuits (e.g., note Malik, paragraph 0009, lines 9-12). It would have been obvious to one of ordinary skill in the art to incorporate Devries' HBT into an optical interconnection circuit because Malik shows that HBTs are of great interest for utilization in such a circuit.

Conclusion

11. The new grounds of rejection presented in this Office action were not necessitated by any amendment(s) filed by the applicant, accordingly, this action is made Non-Final.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903. The examiner can normally be reached on Mon. - Thur. (4-12 hours between 5:30AM and 10 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lex Malsawma
January 7, 2006

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800